Figure 1

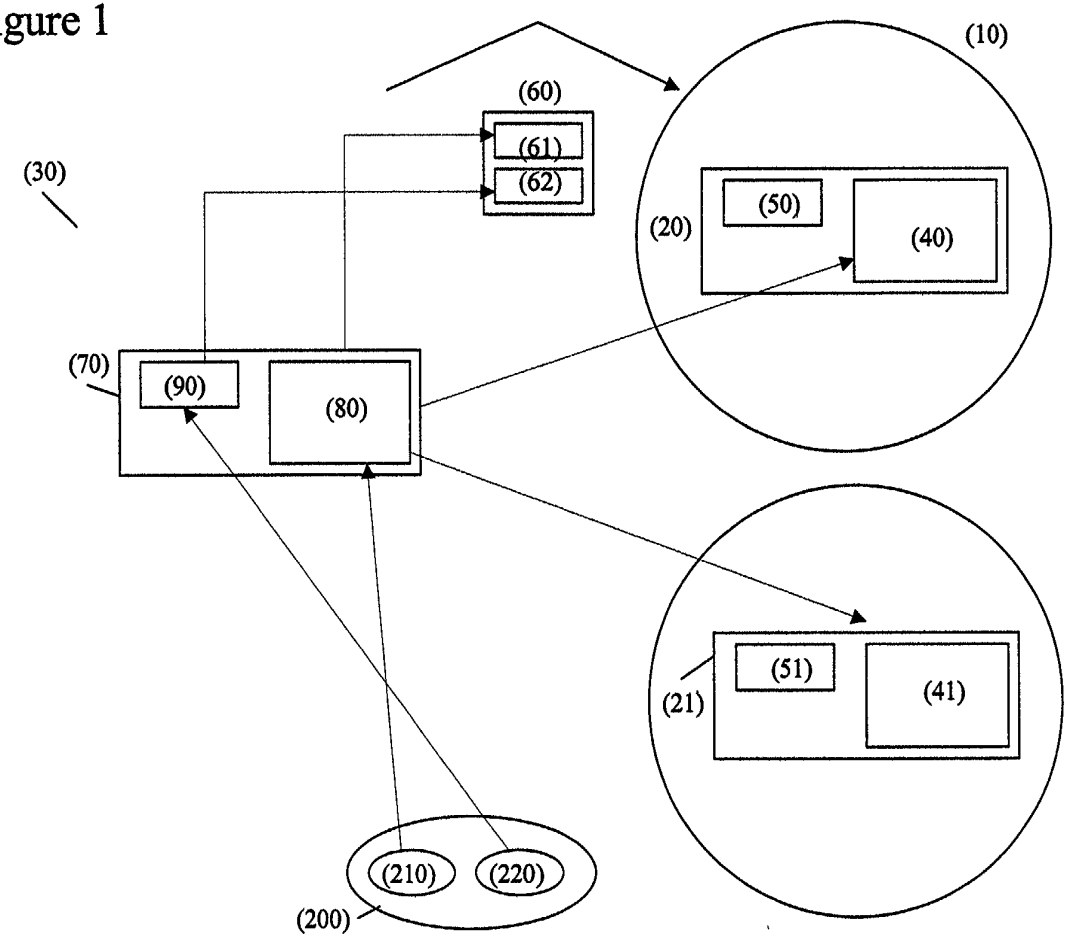
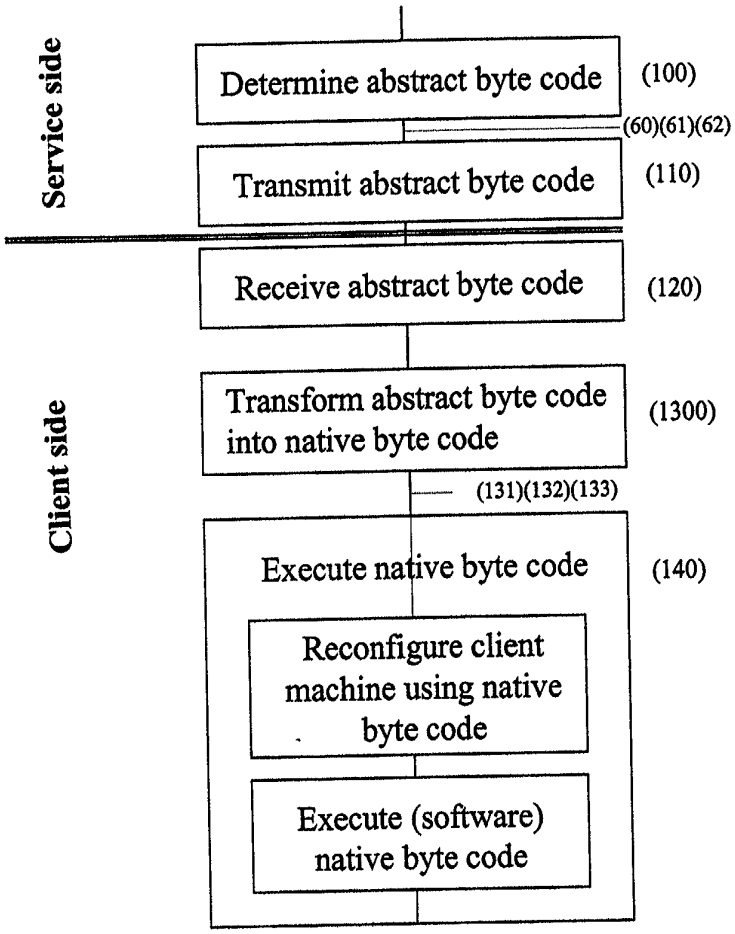


Figure 2



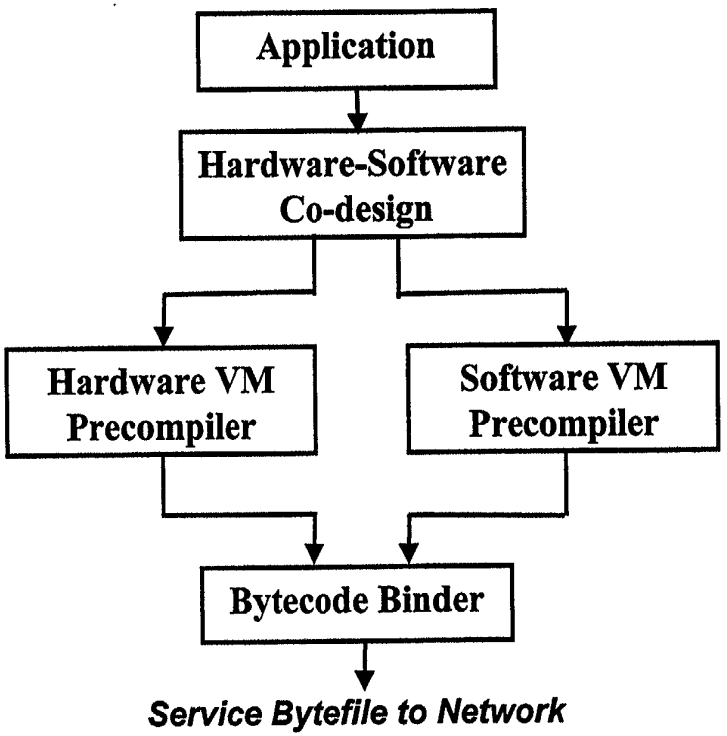

Application
Hardware-Software Co-design
Hardware VM Precompiler
Software VM Precompiler
Bytecode Binder
Service Bytefile to Network

Figure 3

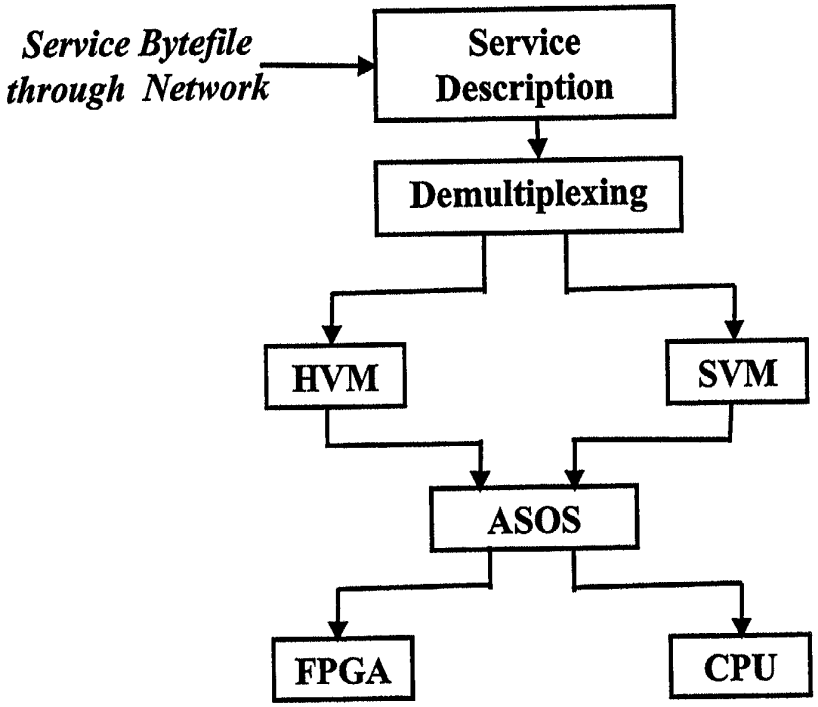


Figure 4

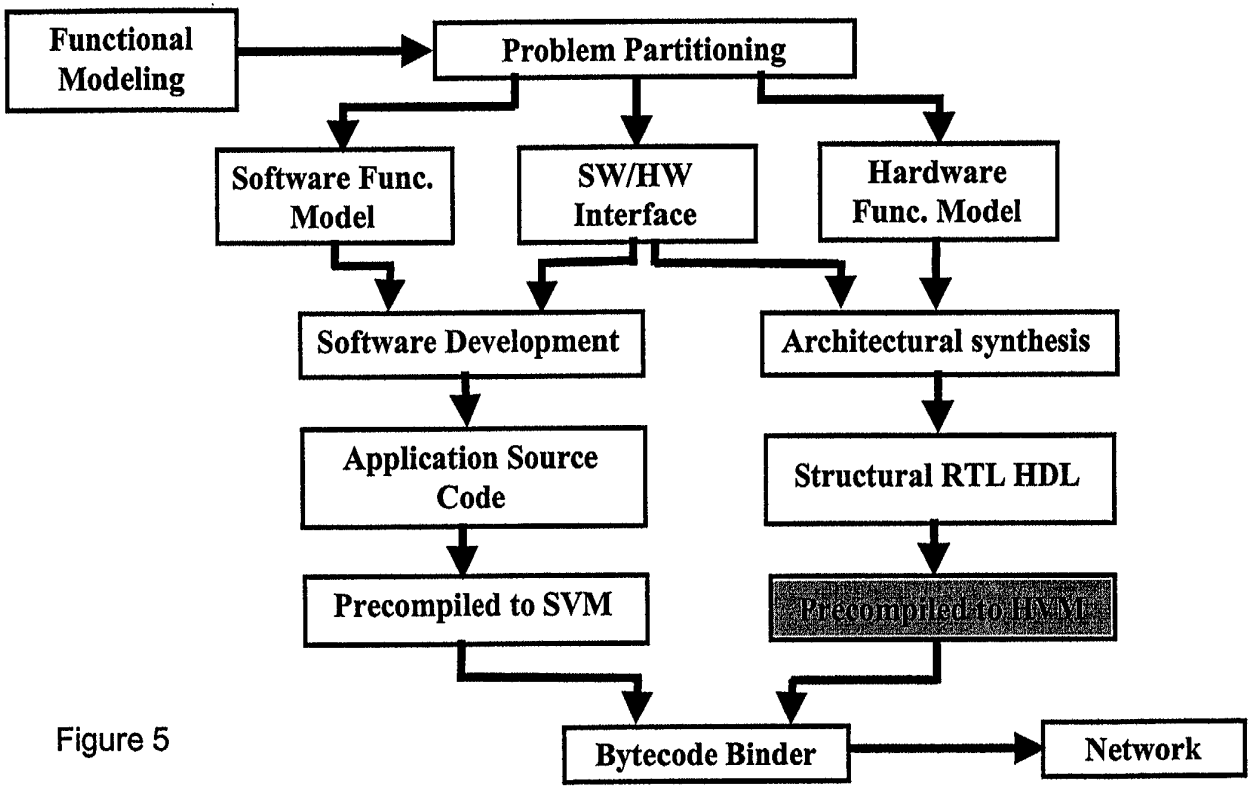

Functional Modeling
Problem Partitioning
Software Func. Model
SW/HW Interface
Hardware Func. Model
Software Development
Architectural synthesis
Application Source Code
Structural RTL HDL
Precompiled to SVM
Precompiled to HVM
Bytecode Binder
Network

Figure 5

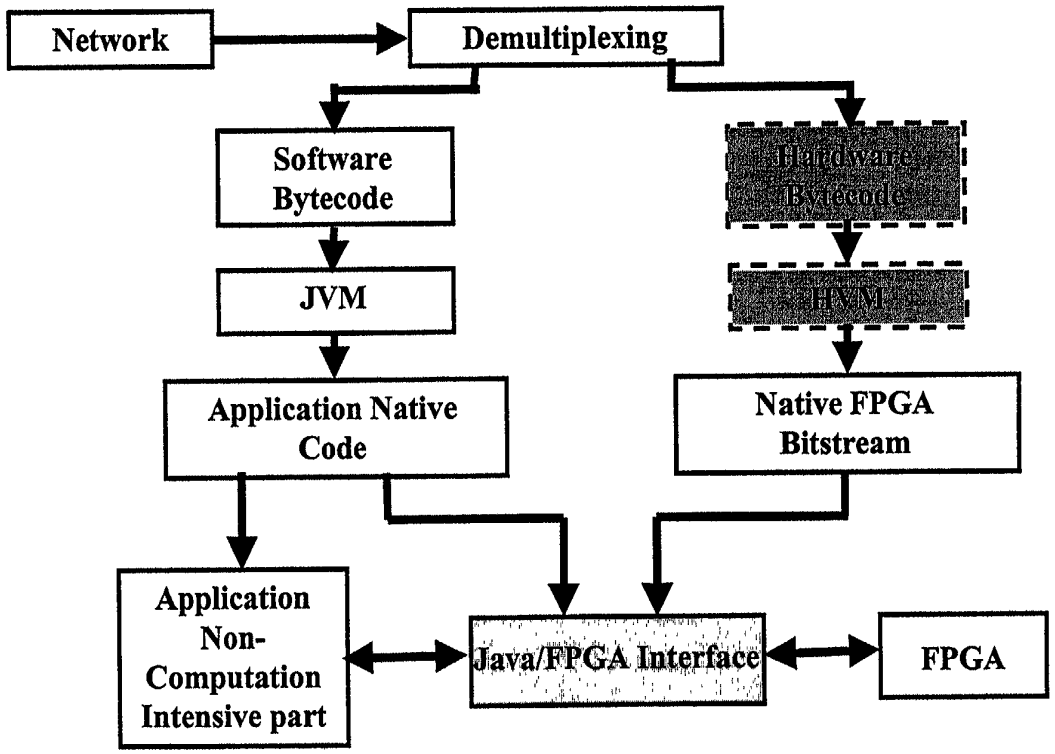

Network
Demultiplexing
Software Bytecode
Hardware Bytecode
JVM
HVM
Application Native Code
Native FPGA Bitstream
Application Non-Computation Intensive part
Java/FPGA Interface
FPGA

Figure 6

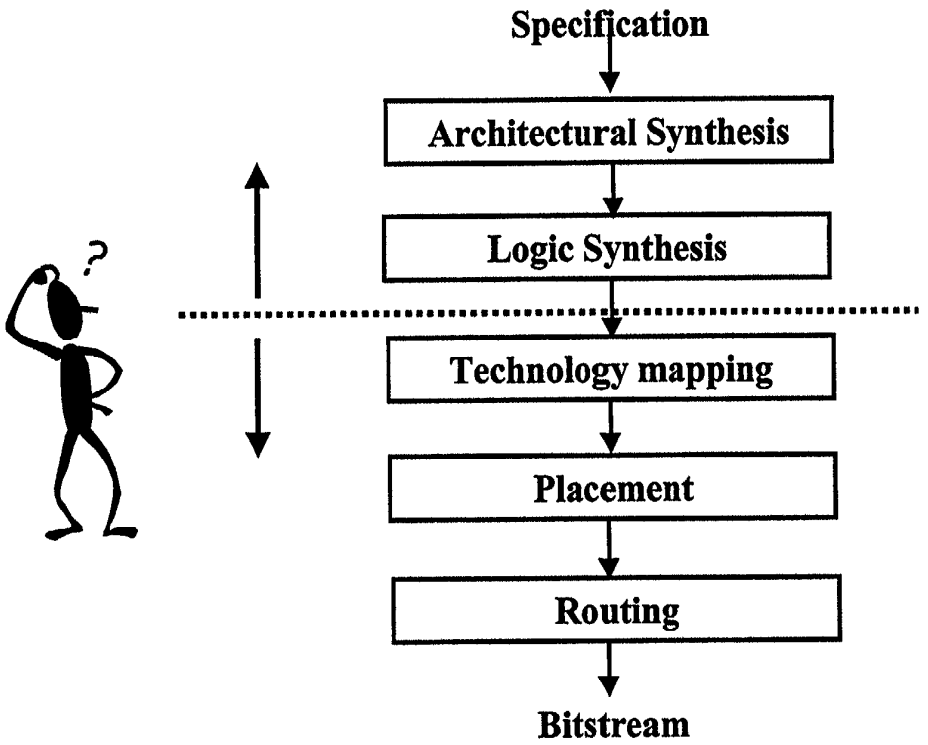

Specification
Architectural Synthesis
Logic Synthesis
Technology mapping
Placement
Routing
Bitstream
?

Figure 7

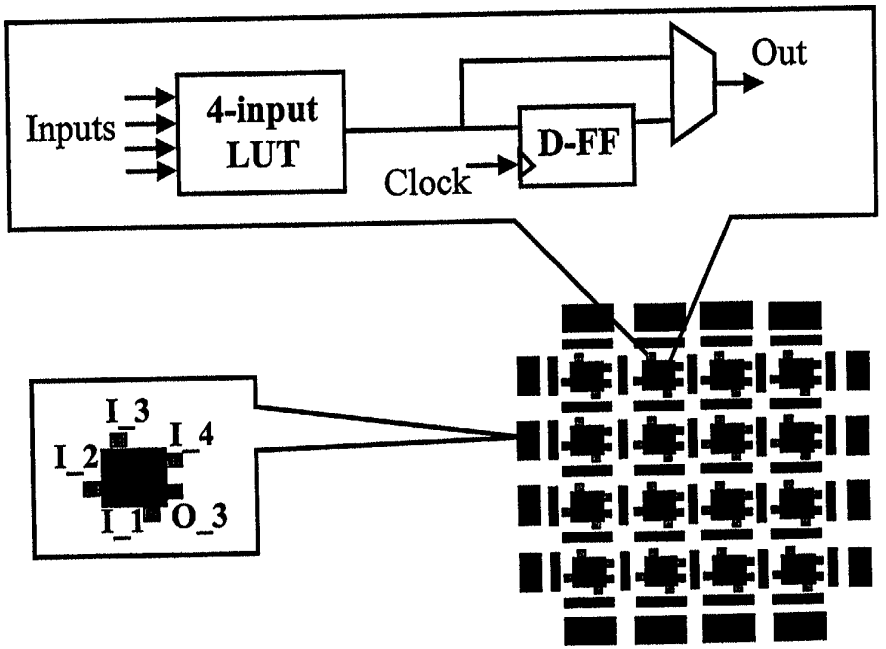


Figure 8

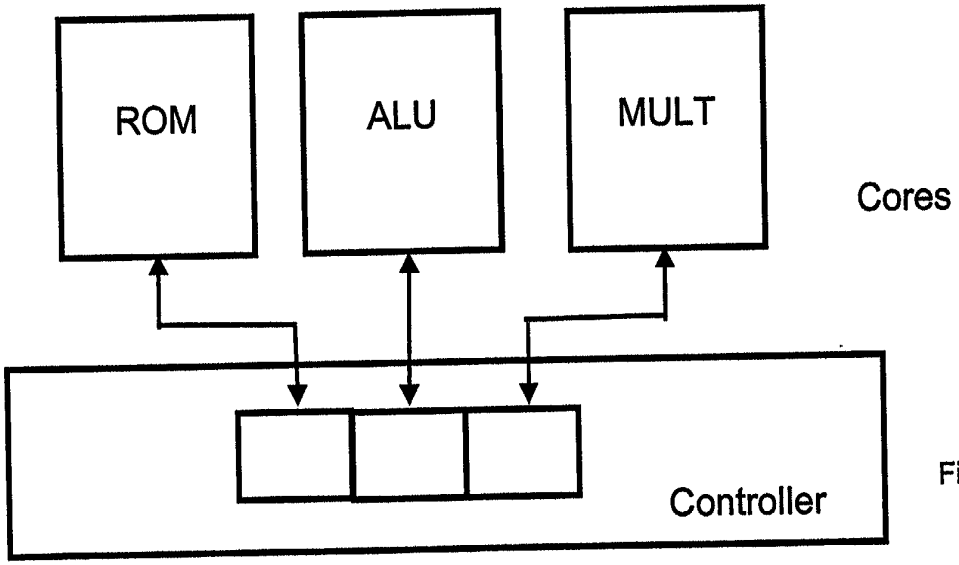


Figure 9

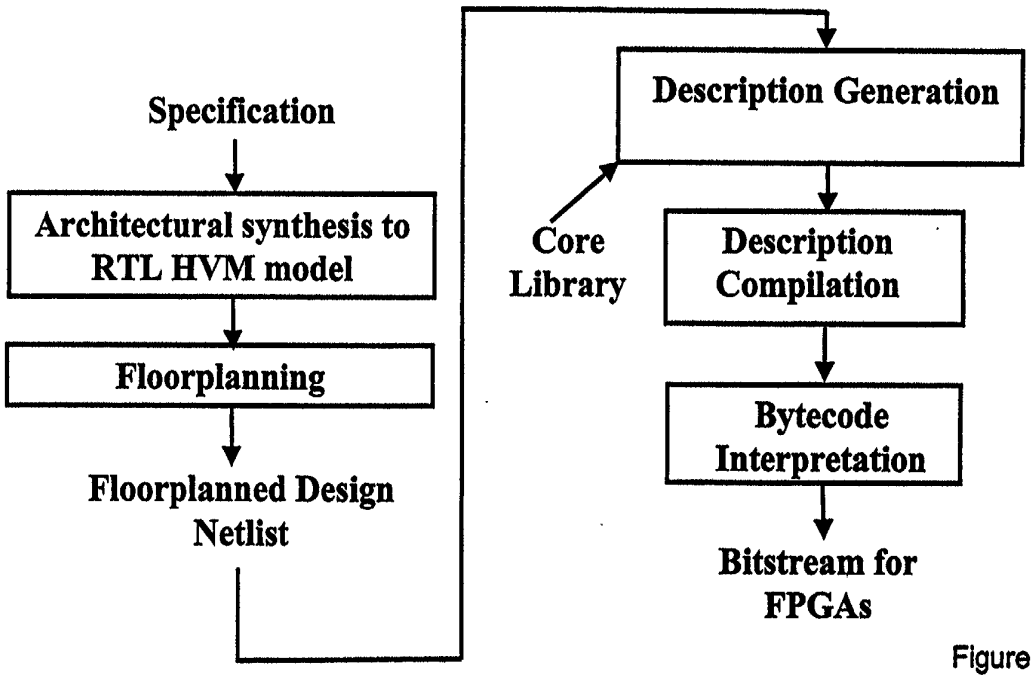

Specification
Architectural synthesis to RTL HVM model
Floorplanning
Floorplanned Design Netlist
Service Provider's Side
Description Generation
Core Library
Description Compilation
Bytecode Interpretation
Bitstream for FPGAs
Client's Side

Figure 10

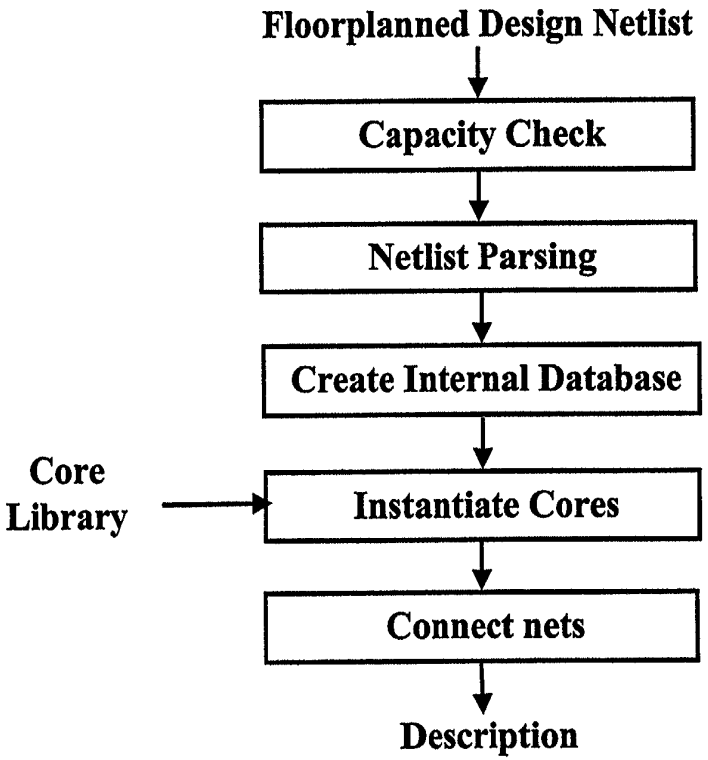

Floorplanned Design Netlist
Capacity Check
Netlist Parsing
Create Internal Database
Core Library
Instantiate Cores
Connect nets
Description

Figure 11

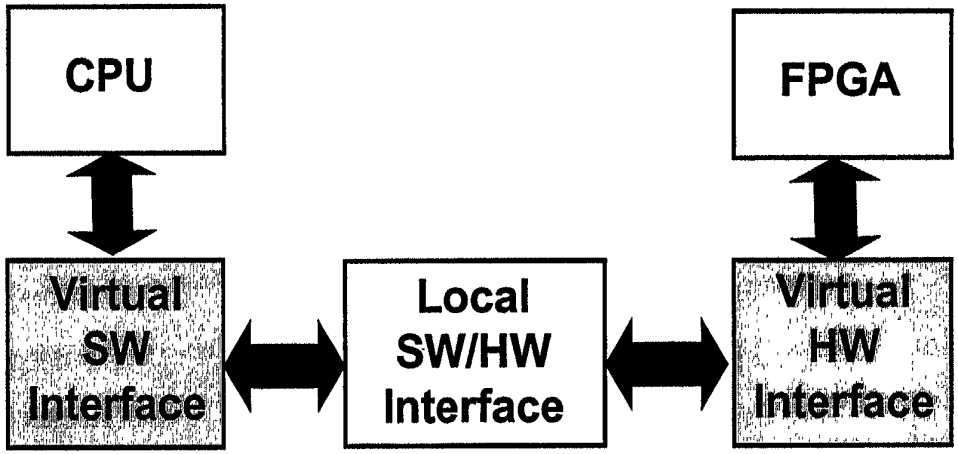

CPU
FPGA
Virtual SW Interface
Local SW/HW Interface
Virtual HW Interface

Figure 12

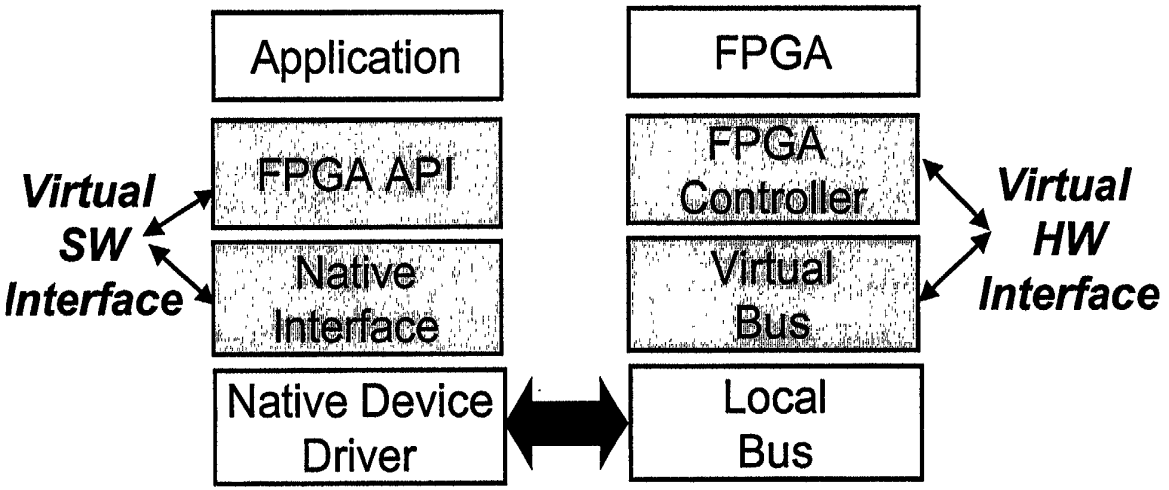

Application
FPGA
FPGA API
FPGA Controller
Virtual SW Interface
Native Interface
Virtual Bus
Virtual HW Interface
Native Device Driver
Local Bus

Figure 13

An Abstract FPGA Model

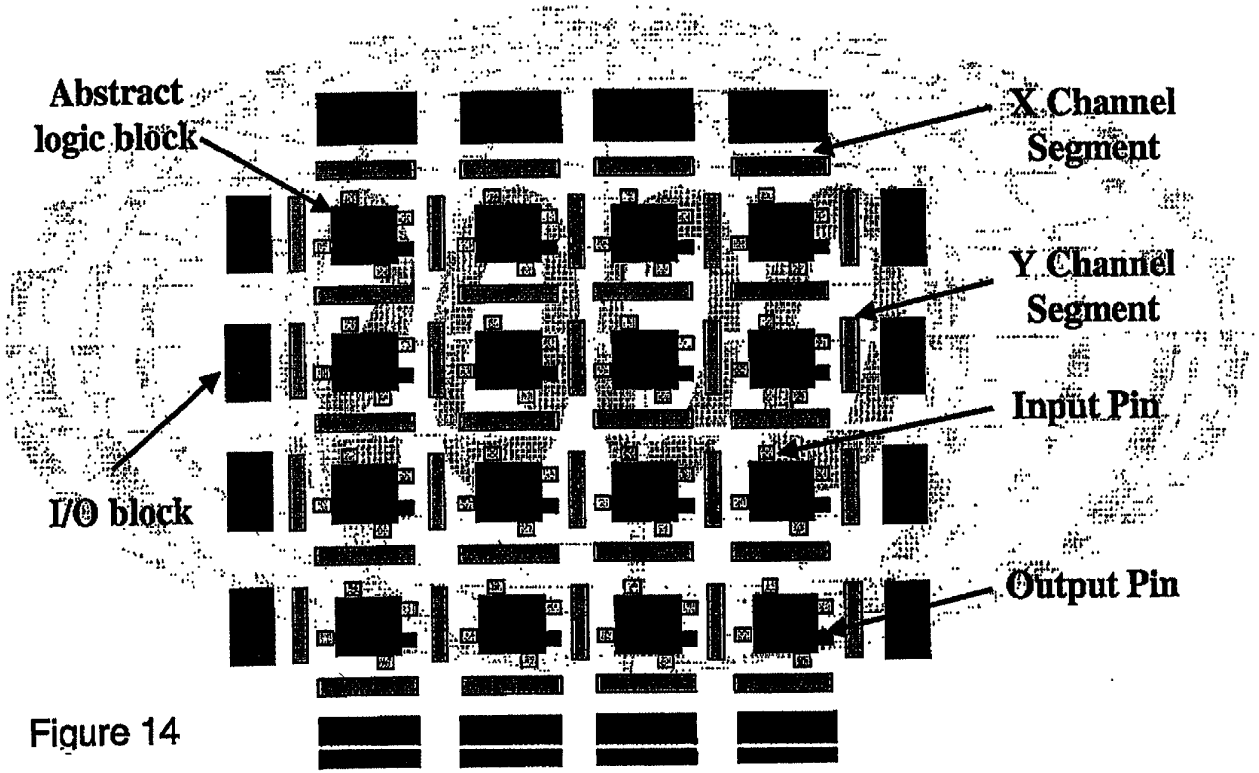


Figure 14